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CONFIRMATION NO. 9419

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SERIAL NUMBER 09/807,500	FILING DATE 06/11/2001 RULE	CLASS 708	GROUP ART UNIT 2124	ATTORNEY DOCKET NO. 851663.422USPC
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APPLICANTS

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** CONTINUING DATA

CD..... verified

This application is a 371 of PCT/SG98/00082 10/13/1998

** FOREIGN APPLICATIONS

CD..... none

Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no	STATE OR	SHEETS	TOTAL	INDEPENDENT
35 USC 119 (a-d) conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	COUNTRY	DRAWING	CLAIMS	CLAIMS
Verified and Acknowledged  Examiner's Signature	INDIA	12	11	13
CD Initials				

ADDRESS

Seed Intellectual Property Law Group
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TITLE

Area efficient realization of coefficient architecture for bit-serial fir, iir filters and combinational/sequential logic structure with zero latency clock output

FILING FEE	FEES: Authority has been given in Paper	<input type="checkbox"/> All Fees
RECEIVED	No. _____ to charge/credit DEPOSIT ACCOUNT	<input type="checkbox"/> 1.16 Fees (Filing)
1344	No. _____ for following:	<input type="checkbox"/> 1.17 Fees (Processing Ext. of time)
		<input type="checkbox"/> 1.18 Fees (Issue)
		<input type="checkbox"/> Other _____
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